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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/944,500	08/31/2001	David W. Hartwell	15311-2312	2641

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HEWLETT PACKARD COMPANY
P O BOX 272400, 3404 E. HARMONY ROAD
INTELLECTUAL PROPERTY ADMINISTRATION
FORT COLLINS, CO 80527-2400

EXAMINER

TORRES, JUAN A

ART UNIT	PAPER NUMBER
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2631

DATE MAILED: 10/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/944,500

Applicant(s)

HARTWELL, DAVID W.

Examiner

Juan A. Torres

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 16 September 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-16 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-16 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Response to Arguments

Applicant's arguments filed on 09/16/2005 have been fully considered but they are not persuasive.

Regarding claim 1

The Applicant contends, "Vowe fails to disclose a phase-locked loop that receives a first clock signal"

The Examiner disagrees and asserts, that, as indicated in the previous Office action Vowe in his patent tiled "Lock detector circuit for a phase-locked loop" discloses a phase-locked loop circuit that receives the clock signal and outputs a second clock signal (figure 2 input TA, column 5 lines 44-61) "The lock detector circuit LD contains a first and second counter ZA, ZB. A first input clock signal TA is coupled into the first counter ZA. A second input clock signal TB is coupled into the second counter ZB. The first input clock signal TA **may be, for example, the divided-down output clock signal of the phase-locked loop. The second input clock signal TB is the reference clock signal, which is generated by a crystal oscillator**, for example. The two input clock signals TA, TB are respectively coupled in at the clock inputs CLK of the counters ZA, ZB". So it is clear that the first signal TA is coming form a PLL and the second signal is the reference signal generated by the VCO. So it is clearly inherently that the PLL receives a clock signal and output a signal that goes to a counter. For these reasons and the reasons indicated in the previous Office action, the rejection of claim 1 is maintained.

Regarding Claims 5 and 9:

The Applicant contends, "Vowe fails to provide any disclosure for a second clock signal that "is locked to the average frequency of the first clock signal". Indeed, Vowe provides no disclosure any relationship between his two clock signals, TA and TB"

The Examiner disagrees and asserts, that, as indicated in the previous Office action Vowe discloses a phase-locked loop circuit that receives the clock signal and outputs a second clock signal (figure 2 input TA, column 5 lines 44-61) "The lock detector circuit LD contains a first and second counter ZA, ZB. A first input clock signal TA is coupled into the first counter ZA. A second input clock signal TB is coupled into the second counter ZB. The first input clock signal **TA may be, for example, the divided-down output clock signal of the phase-locked loop.** The second input clock signal TB is the reference clock signal, which is generated by a crystal oscillator, for example. The two input clock signals TA, TB are respectively coupled in at the clock inputs CLK of the counters ZA, ZB". So it is clear that the first signal TA is coming from a PLL and the second signal TB is the reference signal generated by the VCO of the PLL. So it is clearly inherently that the PLL receives a clock signal and output a signal that goes to a counter. It is well known that the PLL has a Low Pass Filter LPF that averages the variations of the signal. For these reasons and the reasons indicated in the previous Office action, the rejections of claims 5 and 9 are maintained.

The Applicant contends, "Vowe fails to provide any disclosure for a second clock signal that is responsive to a first clock signal"

The Examiner disagrees and asserts, that, as indicated in the previous Office action Vowe discloses a phase-locked loop circuit that receives the clock signal and outputs a second clock signal (figure 2 input TA, column 5 lines 44-61) "The lock detector circuit LD contains a first and second counter ZA, ZB. A first input clock signal TA is coupled into the first counter ZA. A second input clock signal TB is coupled into the second counter ZB. The first input clock signal **TA may be, for example, the divided-down output clock signal of the phase-locked loop**. The second input clock signal TB is the reference clock signal, which is generated by a crystal oscillator, for example. The two input clock signals TA, TB are respectively coupled in at the clock inputs CLK of the counters ZA, ZB". So it is clear that the first signal TA is coming from a PLL and the second signal TB is the reference signal generated by the VCO of the PLL. So it is clearly inherently that the PLL receives a clock signal and output a signal that goes to a counter. It is well known that the PLL has a Low Pass Filter LPF that averages the variations of the signal. For these reasons and the reasons indicated in the previous Office action, the rejections of claims 5 and 9 are maintained.

Regarding claim 2

The Applicant contends, "Vowe fails to disclose a phase-locked loop that receives a first clock signal"

The Examiner disagrees and asserts, that, as indicated in the previous Office action Vowe inherently discloses an output from the comparator that indicates which counter contains a higher count using the VA and VB comparators with different thresholds (figure 2 blocks VA and VB column 4 line 66 to column 7 line 6) Vowe

discloses "The novel lock detector circuit LD operates as follows: if, during a counting operation, the difference between the counter readings CA and CB is greater than a predetermined threshold value, then the lock signals LOCK_A, LOCK_B at the two outputs of the comparators VA, VB are equal to 0. As a result, the lock signal LOCK at the output of the selection device AE also becomes LOCK =0. The phase-locked loop is set to the non-locked state". The threshold can be zero, so we know which counter has higher count. For these reasons and the reasons indicated in the previous Office action, the rejection of claim 2 is maintained.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-3, 5-7 and 9-16 are rejected under 35 U.S.C. 102(e) as being anticipated by Vowe (US 6114917).

As per claim 1 Vowe discloses a error detection system for a clock signal comprising: a first counter that receives and counts the clock signal (figure 2 block ZA, column 5 lines 44-61), a phase-locked loop circuit that receives the clock signal and outputs a second clock signal (figure 2 input TA, column 5 lines 44-61), a second counter that receives and counts the second clock signal (figure 2 block ZB, column 5

lines 44-61), and a comparator that receives and compares the outputs of the first and the second counters (figure 2 block VA, column 5 lines 62-64), and an error output from the comparator that is true when the counts of the first and the second counters are unequal (figure 2 signal LOCK_A, column 6 lines 5-11).

As per claim 2 Vowe inherently discloses an output from the comparator that indicates which counter contains a higher count using the VA and VB comparators with different thresholds (figure 2 blocks VA and VB column 4 line 66 to column 7 line 6).

As per claim 3 Vowe discloses means for resetting the counters synchronized to the successful capture of the clock signal by the PLL (figure 2 reset signal of blocks ZA and ZB, column 6 lines 12-21).

As per claim 5 Vowe discloses a method for detecting clock signal errors comprising the steps of: a first counting of the first clock signals (figure 2 block ZA, column 5 lines 44-61), providing a second clock signal with a frequency that is locked to the average frequency of the first clock signal (figure 2 input TA, column 5 lines 44-61), a second counting of the second clock signals (figure 2 block ZB, column 5 lines 44-61), detecting a difference between the first and the second countings (figure 2 block VA, column 5 lines 62-64), and signaling an error (figure 2 signal LOCK_A, column 6 lines 5-11).

As per claim 6 Vowe inherently discloses an output from the comparator that indicates which counter contains a higher count using the VA and VB comparators with different thresholds (figure 2 blocks VA and VB column 4 line 66 to column 7 line 6).

As per claim 7 Vowe discloses the step of synchronizing the two countings (figure 3 block SE column 6 lines 35-38).

As per claim 9 Vowe discloses a system for detecting errors in a first clock signal, the system comprising means for counting the first clock signal (figure 2 block ZA, column 5 lines 44-61); means, responsive to the first clock signal, for generating a second clock signal (figure 2 input TA, column 5 lines 44-61); means for counting the second clock signal (figure 2 block ZB, column 5 lines 44-61); means for comparing the count of the first clock signal with the count of the second clock signal (figure 2 block VA, column 5 lines 62-64); and means for generating an error when the count of the first clock signal differs from the count of the second clock signal (figure 2 signal LOCK_A, column 6 lines 5-11).

As per claim 10 Vowe discloses that the first clock signal has an average frequency (figure 2 input TB, column 5 lines 44-61); and the second clock signal is locked to the average frequency of the first clock signal (figure 2 input TA, column 5 lines 44-61).

As per claim 11 Vowe discloses that the first clock signal has a plurality of rising edges and a plurality of falling edges (figure 2 block ZA and ZB, column 7 lines 46-56); and the means for counting the first clock signal counts one of the rising and falling edges (figure 2 blocks ZA and ZB, column 5 lines 44-61).

As per claim 12 Vowe discloses that the first clock signal has a plurality of rising edges and a plurality of falling edges (figure 2 block ZA and ZB, column 7 lines 46-56);

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and the means for counting the first clock signal counts both the rising and falling edges (column 1 lines 56-62).

As per claim 13 Vowe discloses that the means for generating a second clock signal includes a phase lock loop (PLL) circuit (figure 2 input TA, column 5 lines 44-61).

As per claim 14 Vowe discloses means for determining whether the count of the first clock signal is higher or lower than the count of the second clock signal (figure 2 blocks VA and VB column 6 line 66 to column 7 line 6).

As per claim 15 Vowe discloses that the means for generating a second clock signal includes a phase lock loop (PLL) circuit (figure 2 input TA, column 5 lines 44-61).

As per claim 16 Vowe discloses that the first clock signal has an average frequency (figure 2 input TB, column 5 lines 44-61); and the second clock signal is locked to the average frequency of the first clock signal (figure 2 input TA, column 5 lines 44-61).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 4 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vowe (US 6114917) as applied to claims 1 and 5 above, and further in view of Shibata (US 5822317).

As per claim 4 Vowe discloses claim 1. Vowe doesn't disclose a sender that sends data and the clock signal, the clock signal defined as a forwarding source synchronous clock signal, and a receiver latch that accepts and latches the data therein with the forwarding clock. It is very well known and Shibata discloses that the use of PLL is with a sender that sends data and the clock signal, the clock signal defined as a forwarding source synchronous clock signal and, a receiver latch that accepts and latches the data with the forwarding clock (column 1 lines 30-36). Vowe and Shibata teachings are analogous art because they are from the same field of endeavor. At the time of the invention it would have been obvious to a person of ordinary skill in the art to combine the Phase lock detecting circuit disclosed by Vowe with the sender and receiver system disclosed by Shibata. The suggestion/motivation for doing so would have been to synchronize the sender and receiver clocks (Shibata column 1 lines 30-36). Therefore, it would have been obvious to combine Vowe and Shibata to obtain the invention as specified in claim 4.

As per claim 8 Vowe discloses claim 5. Vowe doesn't disclose sending data and clock signal, wherein the clock signal is a forwarding source synchronous clock signal, receiving the data, and latching the data with the forwarding clock signal. It is very well known and Shibata discloses that the use of PLL is with a sender that sends data and the clock signal, the clock signal defined as a forwarding source synchronous clock signal and, a receiver latch that accepts and latches the data with the forwarding clock (column 1 lines 30-36). Vowe and Shibata teachings are analogous art because they are from the same field of endeavor. At the time of the invention it would have been

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obvious to a person of ordinary skill in the art to integrate the Phase lock detecting circuit disclosed by Vowe in the sender and receiver system disclosed by Shibata. The suggestion/motivation for doing so would have been to synchronize the sender and receiver clocks (Shibata column 1 lines 30-36). Therefore, it would have been obvious to combine Vowe and Shibata to obtain the invention as specified in claim 8.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.


Any inquiry concerning this communication or earlier communications from the examiner should be directed to Juan A. Torres whose telephone number is (571) 272-3119. The examiner can normally be reached on Monday-Friday 9:00 AM - 5:00 PM.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad H. Ghayour can be reached on (571) 272-3021. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Juan Alberto Torres
10-05-2005


KEVIN BURD
PRIMARY EXAMINER